Flasher Board CPLD Functions

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CPLD I/O definition

signal	I/O	reset value	description
addr[5..0]	I		address bus to DOMMB
data[7..0]	I/O		data bus to DOMMB
nWR	I		
nRD	I		
clock	I		clock from DOMMB (20 MHz)
attn	O	0	request attention to DOMMB
DCDCEN	O	0 (TBR)	DC/DC enable
DCDCON	O	0 (TBR)	DC/DC on
MOSI	O	‘Z’ (TBR)	MAX5438 digital pot
SCLK	O	‘Z’ (TBR)	MAX5438 digital pot
nCS	O	‘Z’ (TBR)	MAX5438 digital pot
OneW	I/O	‘Z’	DS2401
pre_trig	I	0	a.k.a. AUX_RESET
LED_ON	O	pre_trig	a.k.a. LIGHTS_OUT
trig	I	0	trigger from DOMMB
TRIGGER	O	trig	Out to flasher
DP[7..0]	O	0x00 (TBR)	data bus to DS1023 (adjustable delay)
LE_DP	O	1 (TBR)	latch enable for DP
L[11..0]	O	“0…0” (TBR)	
MUX0	O	0 (TBR)	
MUX1	O	0 (TBR)	
ENMUXA	O	0 (TBR)	
ENMUXB	O	0 (TBR)	
ENMUXC	O	0 (TBR)	
ENMUXD	O	0 (TBR)	
ENMUXF	O	0 (TBR)	
SDMUX	O	0 (TBR)	

Registers

Address	R/W	Description	Bits definition
addr_status	R	Flasher board status byte	(Undefined)
addr_reset	W	Write any value to this address causes a soft-reset	
addr_cpld_id	R	Flasher board firmware version	= “0x01” (TBR)
addr_spi	W	Write a value to the SPI device	Alternative implementation of SPI (To be implemented)
addr_mode_select	W	Select mode (normal, spi, 1wire)	(bit1, bit0) “xxxxxx00” for mode_normal “xxxxxx01” for mode_spi “xxxxxx10” for mode_spi
addr_dcdc_control	W	dc/dc control (onoff, enable)	bit0 = bit_dcdc_en (enable) bit1 = bit_dcdc_on (on/off)
addr_delay_adjust	W	DP[0..7]	
addr_delay_config0	W	L[0..3]	
addr_delay_config1	W	L[4..7]	
addr_delay_config2	W	L[8..11]	
addr_mux	W	Flasher board multiplexer enable bits	bit0 = bit_mux_0 (MUX0) bit1 = bit_mux_1 (MUX1) bit2 = bit_mux_a (ENMUXA) bit3 = bit_mux_b (ENMUXB) bit4 = bit_mux_c (ENMUXC) bit5 = bit_mux_d (ENMUXD) bit6 = bit_mux_f (ENMUX_Final) bit7 = bit_mux_sd (SDMUX)