Flasher Board CPLD Address Map

2/19/2003 N. Kitamura

Address		
000000	FL_STATUS	Flasher Board Status Register
000001		
.		
.	(Reserved)	
.		
000111		
001000		OWM Command Register*
001001		OWM Data Tx /Rx Register*
001010		OWM Interrupt Register*
001011		OWM Interrupt Enable Register*
001100		OWM Clock Divisor Register*
001101		OWM Slave Select Register
001110		(Reserved)
001111		OWM Write Pulse
010000	SPISR_ADDR	SPI Status Register**
010001	(Reserved)	
010010	(Reserved)	
010011	(Reserved)	
010100	SPICR_ADDR	SPI Control Register**
010101	(Reserved)	
010110	(Reserved)	
010111	(Reserved)	
011000	SPISSR_ADDR	SPI Slave Select Register**
011001	(Reserved)	
011010	(Reserved)	
011011	(Reserved)	
011010	SPITR_ADDR	SPI Transmit Data Register**
011011	(Reserved)	
011110	SPIRR_ADDR	SPI Receive Data Register**
011111	(Reserved)	
100000		
.		
.	(Reserved)	
.		
111111		

*Must be four (4) consecutive addresses (OWM master)

**See XAPP386 (v1.0) Dec 24, 2002, Xilinx documentation.