

## MEMO

### Flasher Board-Main Board Interface Requirements

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This memo contains all the known interface requirements. The contents of sections 3.1.1 thru 3.1.3 of [FlasherboardERD 0.01d](#) are to be updated according to the specifications given here.

#### 1 Mechanical

1. Flasher Board shall be an [annular-shaped circuit board](#).
2. Flasher Board shall be screw-mounted to the [PMT collar](#) at three locations near the ID.
3. Flasher Board shall provide a mechanism for mounting the Main Board underneath it.
4. Flasher Board shall support the weight of the Main Board and the Delay Board.
5. Flasher Board shall provide a board area for the Passive PMT Base support devices.

#### 2 Electrical Connections

1. Flasher Board shall make logic signals, power and ground connections with the Main Board through a board-to-board connector.
  - (a) Said connector is as specified [elsewhere](#).
  - (b) Said connector pinouts are as specified [elsewhere](#).
  - (c) Said connector location and orientation on board are as specified [elsewhere](#).
2. Flasher Board shall make a coaxial-cable connection to the Main Board for the purpose of carrying the flasher timing pulse (defined elsewhere).
  - (a) Said coaxial-connection cable shall be of the type specified elsewhere.
  - (b) Said coaxial-connection shall have a connector, specified elsewhere, on either end.

#### 3 Electrical Power

1. Flasher Board shall receive electrical power from the Main Board.

- (a) Said electrical power source shall be +5V, -5V, +3.3V, +1.8V and +90V.
  - (b) The +5V and -5V sources shall have a voltage uncertainty of no greater than  $\pm 5\%$ .
  - (c) Specifications for the +3.3V source shall be defined elsewhere.
  - (d) Specifications for the +1.8V source shall be defined elsewhere.
  - (e) Specifications for the +90V source shall be defined elsewhere.
2. The combined power consumption by the Flasher Board from the +5V, -5V, +3.3V and +1.8V power sources shall be no greater than (**TBD**).
3. The power consumption of the Flasher Board from the +90V power source shall be no greater than (**TBD**).
4. The entire Flasher Board shall be powered ON or OFF by a single-bit digital command (pin #24) issued by the Main Board.

#### 4 Ground

1. There shall be a common power ground for the low-voltage DC power sources (+1.8V, +3.3V, +5V and -5V).
2. There shall be a separate power ground for the +90V power source (pin #47).
3. Signal ground shall be the same as the power ground for the low-voltage DC power sources.

#### 5 Digital Signals

1. Clock—The Main Board shall provide the clock signals to the Flasher Board.
  - (a) The clock shall be a LVDS differential pair (pins 2, 3).
  - (b) The clock frequency shall be (**TBD**).
  - (c) The clock shall be provided for a general purpose and shall have no definite timing relationship with the rest of the digital signals. (Note: Specifically, no clear timing relationship with nWR and nRD.)
2. Digital signal standard—The digital signals, other than the clock signals, shall comply with the 3.3V CMOS standard.
3. Digital communication
  - (a) Flasher Board shall digitally communicate with the Main Board using the following signals:
    - A 6-bit-wide address bus
    - An 8-bit-wide data bus
    - An active-low read strobe (nRD)

- An active-low write strobe (nWR)
  - (b) The Main Board shall serve as the bus master and control the read strobe signal and the write strobe signal.
  - (c) The timing specifications for the bus communication shall be given elsewhere.
  - (d) Flasher Board shall be allowed to issue an interrupt to the Main Board by asserting an appropriate signal (pin 36, ATTN).
4. LED Flasher Control Signals
- (a) Pre-trigger—The Main Board shall assert this signal at least (**TBD**) seconds prior to issuing the trigger command.
  - (b) Trigger—The trigger command issued by the Main Board shall be a differential pair of digital signals, each signal of the pair complying with the same standard as the rest of the digital signals.
5. JTAG—The Flasher Board firmware shall be programmable by the Main Board.
- (a) The supported JTAG signals shall be TCK, TDO, TDI and TMS.
  - (b) Flasher Board shall provide a pull-up resistor for the JTAG signals.
  - (c) The JTAG ports shall be enabled for programming when the Main Board asserts JTAG\_EN signal pin (pin #33).

## 6 Logical and Functional

1. Flasher Board shall have an internal address space that is accessible by the Main Board.
2. Said address space shall be accessible using the address bus, the data bus, read strobe and write strobe, defined above.
3. Said address space is as defined [elsewhere](#).
4. Each address location is readable, writable or both for the Main Board.
5. All the functionality of the Flasher Board shall be controlled by the Main Board, according to a predefined sequence of write operations to and read operations from the internal address space of the Flasher Board.
6. The sequences of read and write operations required to operate the Flasher Board for individual functionality shall be carried out by a program code running on the Main Board.