Flasher Board CPLD Pin Assignment

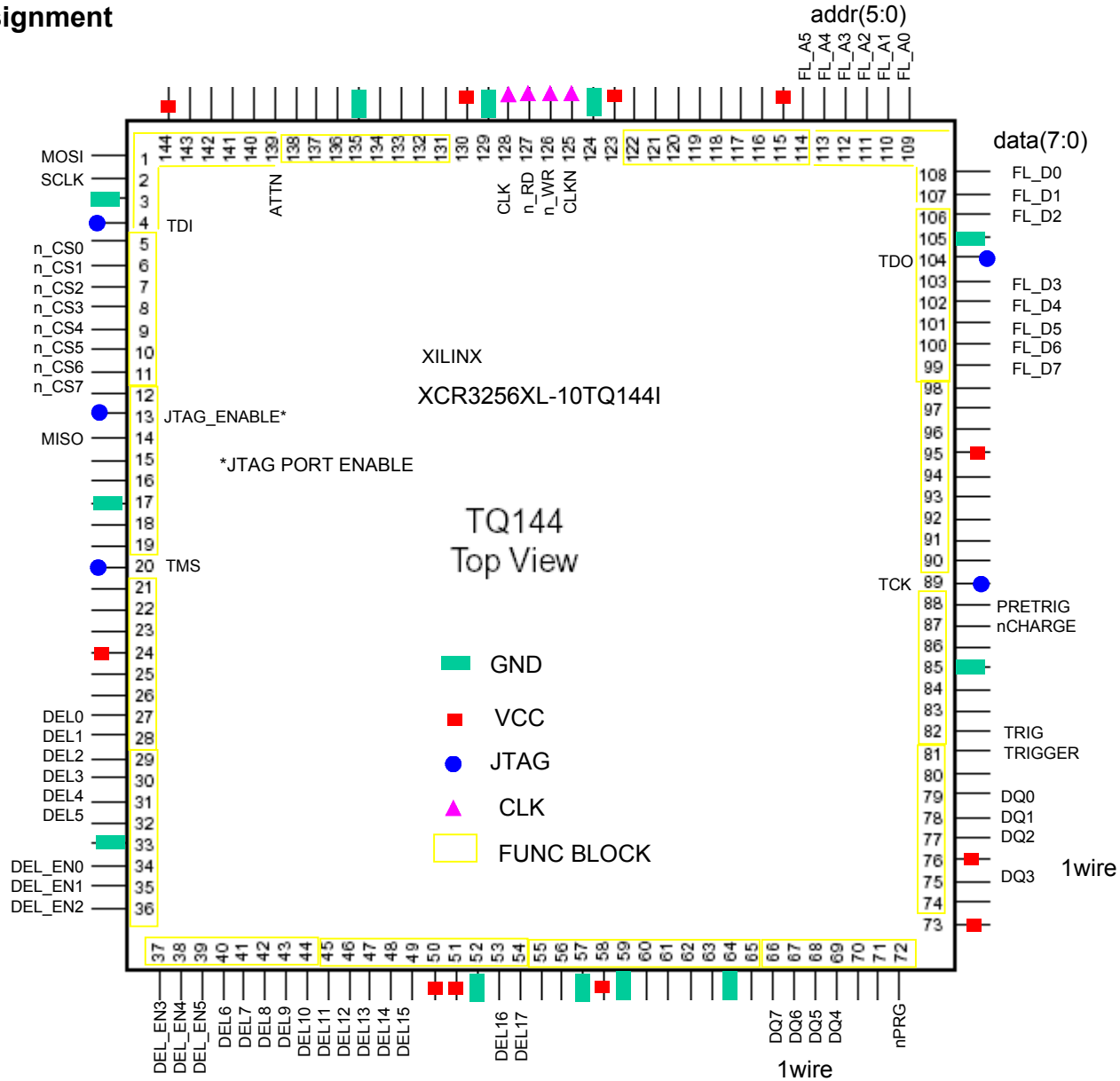
JTAG Port
JTAG_ENABLE (PIN#13) must be “low” for normal operation; “high” for in-system programming. NK recommends a resister pull-down.

JTAG pins (4, 20, 89, 104) need a 10KOhm pull-up in a noisy environment.

1-Wire Devices
DQ(0..5)→ DS2502 (PROM)
DQ(6)→ DS2401 (Board ID)
nPRG provides active-low programming pulse (see next page)

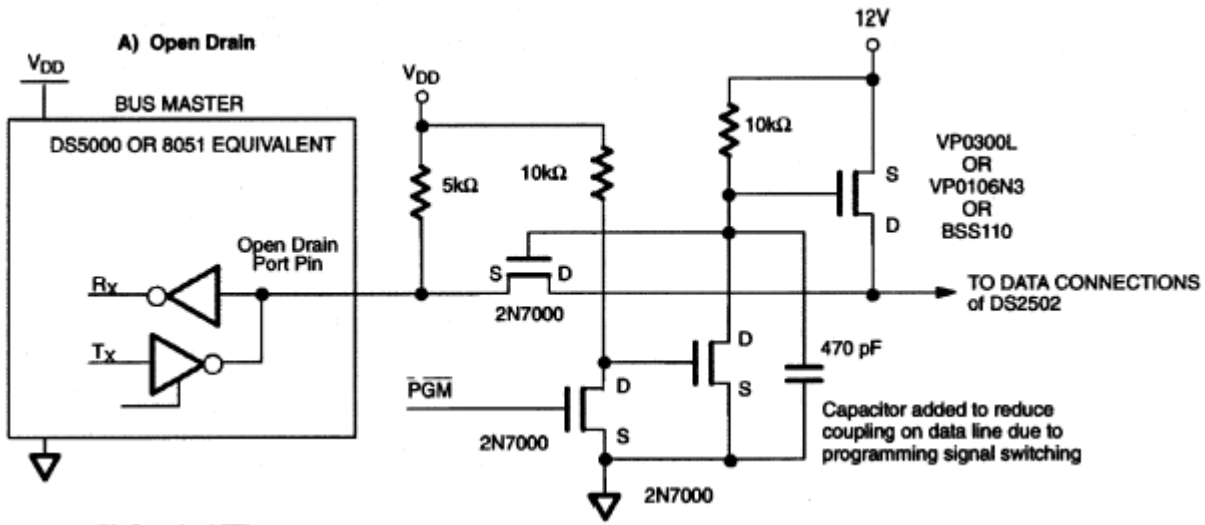
SPI
n_CS6, n_CS7 and MISO are not assigned to any device at this time.

Adjustable Trigger Delay
DEL(17:0) is divided into six groups of three bits each. Each group is assigned one of DEL_EN(5:0) used as an enable.



DS2502 Programming Circuit

In order to allow the DS2502 devices to be programmable, each corresponding must have a programming circuit similar to what is shown below. Pin #72 (nPRG) provides the programming pulse (active low).
A demulplexer, internal to the CPLD, selects a desired 1-Wire device. The devices are not connected to a single 1-Wire bus, in order to simplify the read-out software.



DS2502 datasheet, page 15
(http://www.ssec.wisc.edu/~kitamura/NK/Datasheets/Dallas_1Wire/)